TRI-STATE® 64-Bit Random Access Memories

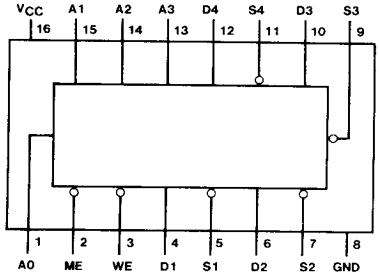
General Description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four address inputs. After addressing, information may be either written into or read from the memory. To write, both the memory enable and the write enable inputs must be in the logical "0" state. Information applied to the four write inputs will then be written into the addressed location. To read information from the memory the memory enable input must be in the logical "0" state and the write enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the memory enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus line without the use of pull-up resistors. All memories except one are gated into the high impedance state while the one selected memory exhibits the normal low impedance output characteristics of TTL.

Features

- TRI-STATE outputs
- Same pin-out as DM5489/DM7489
- Organized as 16, 4-bit words
- Expandable to 2048, 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns

Connection Diagram

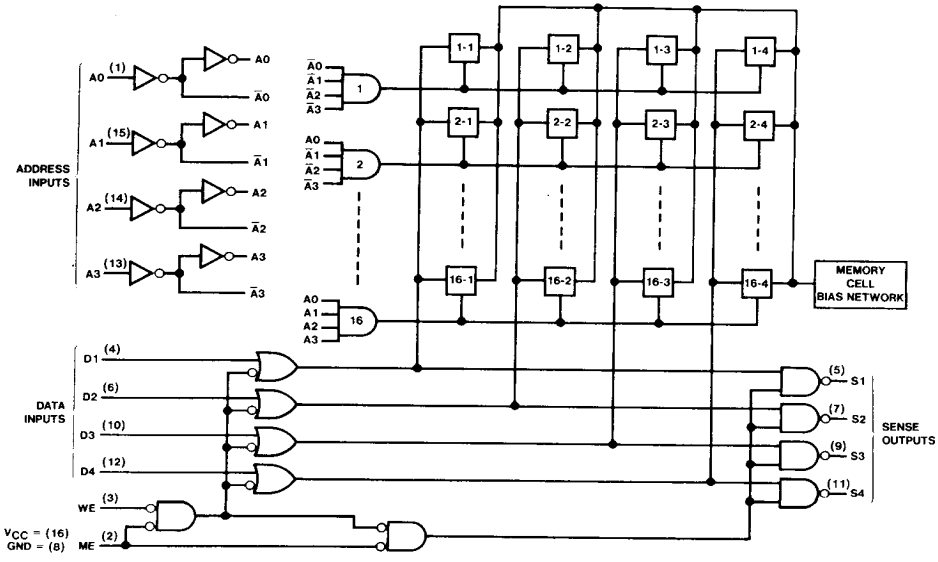


7599 (J); 8599 (N)

Truth Table

Memory Enable	Write Enable	Operation	Outputs
L	L	Write	Hi-Z
L	H	Read	Complement of Data Stored in Memory
H	X	Hold	Hi-Z

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM75/85 99 Min	DM75/85 99 Typ (1)	DM75/85 99 Max	Units
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0	mA
			DM85			−5.2	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = Max				2.4	V
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4 V			−40	μA
			V_O = 2.4 V			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	120	mA

Note 1: All typical values are at V_{CC} = 5 V and T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter			From (Input)	To (Output)	Conditions	DM75/85 99 Min	DM75/85 99 Typ	DM75/85 99 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Address	Output	C_L = 50 pF, R_L = 400 Ω		27	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Address	Output			28	45	ns
t_{ZH}	Output Enable Time to High Level		ME	Output			14	20	ns
t_{ZL}	Output Enable Time to Low Level		ME	Output			19	30	ns
t_{HZ}	Output Disable Time from High Level		ME	Output	C_L = 5 pF, R_L = 400 Ω		12	20	ns
t_{LZ}	Output Disable Time from Low Level		ME	Output			21	30	ns
t_{SETUP}	Setup Time	Address				0	17		ns
		Data				0	−15		ns
t_{HOLD}	Hold Time	Address				5	−7		ns
		Data				0	−14		ns
t_{WP}	Write Enable Pulse Width					40	23		ns
t_{SR}	Sense Recovery Time						42	60	ns

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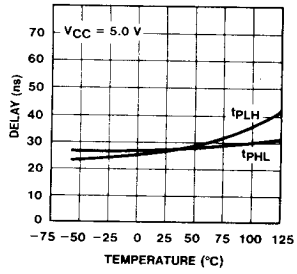
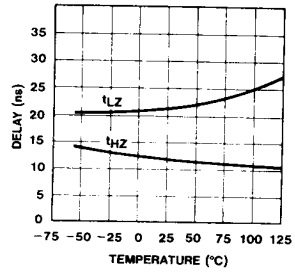
Typical Performance Curves

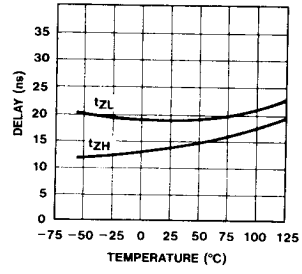
Delay From Address To Output



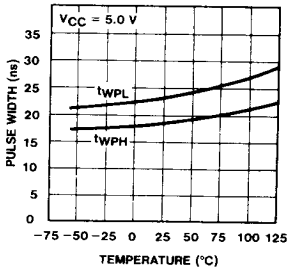
Delay From Enable To High Impedance State



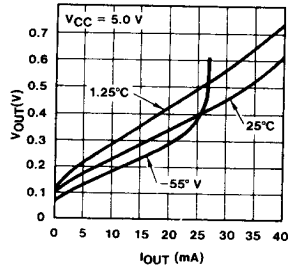
Delay From Enable To Low Impedance State



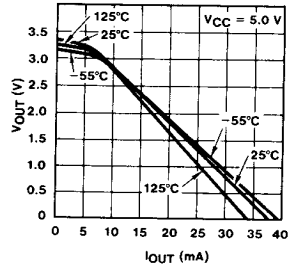
Minimum Write Pulse Width



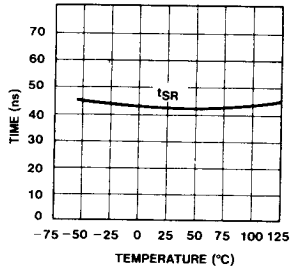
Logical "0" Output Voltage vs Sink Current



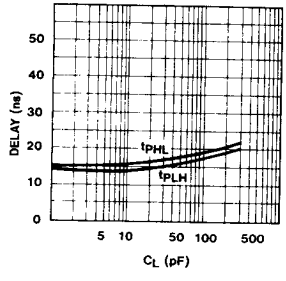
Logical "1" Output Voltage vs Source Current



Sense Recovery Time

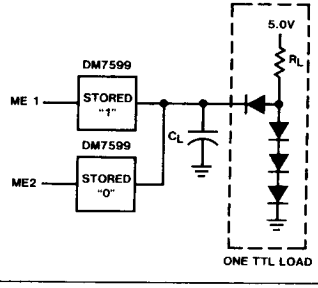


Delay From Enable To Output vs Load Capacitance



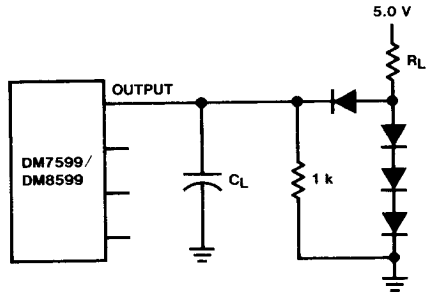
Test Circuit

Test Circuit For Delay Vs Load Capacitance



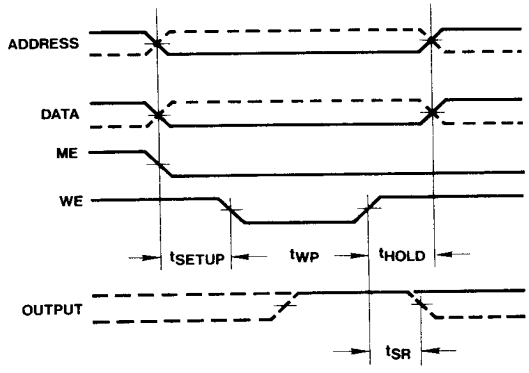
Note: In a typical application the output of the TRI-STATE memories might be wired together and one would be switching to the low impedance state at the same time the circuit previously selected would be switching back into the high impedance state. The measurements of delay versus load capacitance were made under conditions which simulate actual operating conditions in an application. (See test circuit.)

AC Test Circuit

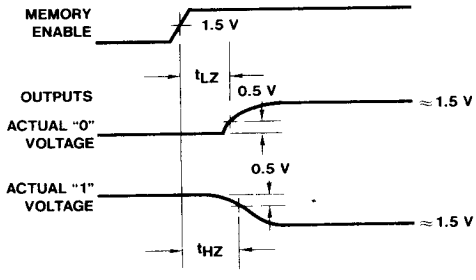


Switching Time Waveforms

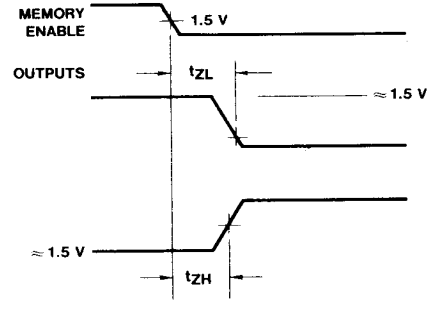
WRITE CYCLE



t_{LZ} & t_{HZ}



t_{ZL} & t_{ZH}



Note: The pulse generator has the following characteristics: V = 3.0 V, t_r = 15 ns, t_f = 5.0 ns, f = 500 kHz, duty cycle = 50%, Z_{OUT} = 50 Ω, V_t = 1.3 V @ 25°C.

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